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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,371	02/26/2004	YI-JEN CHAN	11955-US-PA	2370

31561 7590 06/14/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
NGUYEN, LINH V	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,371	CHAN ET AL.	
	Examiner	Art Unit	
	Linh V. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application No. 10/708,371 filed on 02/26/2004. Claims 1 – 15 are pending on this application.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 - 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsunaga et al. U.S. Patent No. 6,759,906.

Regarding claim 1, Fig. 1 of Matsunaga et al. discloses a power amplifier with an active bias circuit (10), comprising: a power amplifier transistor (Q1) with a gate (gate of Q1) connected to a gate bias voltage (Vg1); and an active bias circuit (10) connected

to an input power terminal (Vapc) and the gate of the power amplifier transistor (gate of Q1) for receiving an input power from the input power terminal (Vapc) and outputting the gate bias voltage (Vg1), to the gate wherein the gate bias voltage (Vg) is increased corresponding to an increase (See Fig. 2) of the input power (Vapc).

Regarding claim 2, wherein a curve of an increase of the gate bias voltage versus the input power is a linear curve (Fig. 2).

Regarding claim 3, wherein a curve of an increase of the gate bias voltage versus the input power is a non-linear curve (Fig. 2).

Regarding claim 4, wherein the power amplifier transistor and the active bias circuit is manufactured by a system on chip process (Col. 8 lines 53 – 54).

Regarding claim 5, wherein the active bias circuit comprises a diode (See Fig. 7 discloses an active bias circuit 10 of Fig. 1 having a diode Q14, Q22 and a resistor (R11 – 13).

Regarding claim 6, wherein an equivalent resistance of the diode in the active bias circuit varies in correspondence with the input power (this is an inherent characteristic of diode transistor Q12 and Q14, because the equivalent resistance value of diode transistor is depended upon of the power voltage input of Vapc).

Regarding claim 7, Fig. 1 of Matsunaga et al. discloses an integrated circuit for a power amplifier with an active bias circuit (10), comprising: a power output device (Vapc); a power amplifier transistor (Q1) with a gate connected to a gate bias voltage (Vg1); an active bias circuit (10) connected to the power output device (Vapc) and the gate of the power amplifier transistor (Q1) for receiving an input power (Vapc) from the

power output device and providing a gate bias voltage (Vg) to the gate (gate of Q1), wherein the gate bias voltage (Vg) is increased corresponding to an increase of the input power (Vapc); and a power input device (Q2) connected to an output terminal of the power amplifier transistor (Q1) for receiving an amplified output power from the power amplifier transistor (Q1).

Regarding claim 8, wherein a curve of an increase of the gate bias voltage versus the input power is a linear curve (Fig. 2).

Regarding claim 9, wherein a curve of an increase of the gate bias voltage versus the input power is a non-linear curve (Fig. 2).

Regarding claim 10, wherein the power amplifier transistor and the active bias circuit is manufactured by a system on chip process (Col. 8 lines 53 – 54).

Regarding claim 11, wherein the active bias circuit comprises a diode (See Fig. 7 discloses an active bias circuit 10 of Fig. 1 having a diode Q14, Q22 and a resistor (R11 – 13).

Regarding claim 12, wherein the equivalent resistance of the diode in the active bias circuit varies in correspondence with the input power (this is an inherent characteristic of diode transistor Q12 and Q14, because the equivalent resistance value of diode transistor is depended upon of the power voltage input of Vapc).

Regarding claim 13. Fig. 1 of Matsunaga et al. discloses method for generating a gate bias voltage (Vg) of a power amplifier transistor 9Q1) corresponding to an input power (Vapc), comprising: providing an input power (Vapc); and outputting a gate bias

voltage (Vg1) corresponding to the input power (Vapc), wherein the gate bias voltage is increased corresponding to an increase of the input power (Fig. 2).

Regarding claim 14, wherein a curve of an increase of the gate bias voltage versus the input power is a linear curve (Fig. 2).

Regarding claim 15, wherein a curve of an increase of the gate bias voltage versus the input power is a non-linear curve (Fig. 2).

Contact Information

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Robert Pascal can be reached at (571) 272-1769. The fax phone numbers for the organization where this application or proceeding is assigned are (703-872-9306) for regular communications and (703-872-9306) for After Final communications.

6/9/05

Linh Van Nguyen

Art Unit 2819